The goal of the Memory Wall Project is to improve memory system performance for Symmetric Multiprocessors (SMP) by improving the current utilization of cache memory. To help us achieve this goal we are building a simulator that will allow us to try out ideas on how to utilize the cache better. After the simulator is completed, tests will be run to find ideas that will be worth trying in hardware. Currently we have validated the cache memory simulation component in a single processor environment for L1 and L2 caches. Next we will be building the foundation for a simulation that will be capable of modeling a more complicated machine.